Diamond

CVD Thin-Film Process / CMOS Device — Hybrid R&D Engineer

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Career Objective

CMOS device development / TD process-device integration — open to all locations in China; values career growth and compensation level.

Summary

11 years of full-chain semiconductor R&D; dual background in CVD thin-film process and CMOS/TFT/3D NAND devices; complete hands-on experience across a leading memory maker, a display-panel maker and a specialty-process foundry — strong at resolving device electrical anomalies, reliability degradation and mass-production failures from the thin-film level.

Pursuing a PhD in IC Engineering (a top-985 university in Wuhan) while working — combining industrial experience with frontier theory: TCAD simulation, DFM co-design and PDK modeling.

60+ invention patents as first inventor (5 granted, rest under substantive examination), spanning four directions: advanced CMOS, TFT, 3D-memory device structures and novel CVD thin-film processes; outstanding continuous-innovation and independent problem-solving ability.

Full-chain capability across device development, TD process integration, PIE yield ramp and process-design (DFM) co-optimization; unlike a single-process role, can independently own end-to-end device R&D.

Core Skills

Device Development Core

- CMOS/MOS full-flow device R&D
- Process-device correlation modeling (TCAD/DFM/PDK)
- Electrical & reliability analysis (HCI/NBTI/PBTI)

CMOS/MOS full-flow device R&D: structure design, DC/AC/transient electrical test, threshold/leakage/noise/reliability analysis (HCI, NBTI, PBTI).

TFT/LTPO/3D NAND device failure analysis, lifetime & voltage-withstand iteration; high-k gate dielectric and interface-passivation optimization.

TCAD Sentaurus/Silvaco process & device simulation, stress simulation, device SPICE extraction; process-device co-optimization, DFM risk control, PDK-assisted modeling.

CVD Thin-Film & TD/PIE Integration

Film uniformity / step coverage / stress

Process-window dev. & SPC control

Defect suppression & yield improvement

Proficient in PECVD, HDP and ALD dielectric-film development, recipe tuning, equipment-abnormal handling and mass-production ramp.

TD process integration: film/etch/implant/anneal full-flow linkage; cross-functional PIE/device/design co-advancement.

Mass-production yield improvement, defect root-cause analysis, SPC control, process cost-down, domestic-equipment adaptation.

Tools & General

Simulation / test (TCAD/Silvaco/Origin)

Language / technical reporting (CET-6)

Project management / patent portfolio

Simulation/office: Silvaco TCAD, Origin, AutoCAD, full Office suite.

Language: CET-6 — fluent in reading English literature and independently writing CN/EN technical reports.

Project management: independently leading R&D projects, DOE design, patent mining & portfolio; 60+ first-author invention patents.

Work Experience

Specialty-Process Foundry

2023.4 — present

CVD Process Development Engineer

- Owned advanced-logic (28/40/55nm) / power-device (90BCD) CVD thin-film R&D, mass-production iteration and yield improvement; concurrently handled CMOS device electrical tuning and process-device matching verification.
- Led new-process development and mass-production introduction of the full CVD family (HARP, OX, SIN, HDP, ALD), resolving uniformity, interface defects, stress, particle/bump defects and wafer arcing — significantly lifting yield and long-term reliability.
- Deeply collaborated with device/PIE teams to iterate CMOS and power-device film stacks, optimize interface passivation, and improve threshold drift, leakage, short-channel effects, noise and voltage-withstand degradation.
- Built a process-parameter to device-electrical correlation database and a variation-impact model, supporting PDK extraction, DFM risk prediction and TD integration optimization.
- Led technical innovation and IP portfolio — 50+ first-author invention patents during the current stint.

- Advanced domestic-equipment adaptation, tool WPH optimization and process cost-down, landing multiple stable mass-production film processes.

Leading Domestic Memory Maker (3.7 yrs)

2015.7 — 2023.3

3D NAND CVD Process & Device R&D Engineer

- Full-process participation in 3D NAND from "0" to "1" and 32/64/128/196-layer iteration, with complete project and iteration experience.
- Proficient in the full CVD suite (OX, SIN, TEOS, HDP, carbon film, ALD); owned 3D NAND new-product process R&D and collaborated with PIE on yield ramp and domestic-equipment validation.

Display Panel Maker (4 yrs)

2015.7 — 2023.3

TFT Device R&D Engineer

- Improved TFT stability via thin-film interface-defect control; applied four-point-probe testing to analyze MOS hysteresis, NBTI, PBTI and HCI effects.
- Used TCAD stress simulation to converge panel-device failures: film-stress mismatch, panel cracks, image retention and FOD Mura.

Education

Top-985 University in Wuhan

2024.9 — present

IC Engineering | PhD (in progress) | 2024.9 — present

- Research: advanced CMOS device-structure optimization, process-device co-modeling, device reliability and PDK parameter calibration; deep in the Fab-manufacturing × IC-design cross-domain; systematic command of device physics, TCAD simulation and DFM co-design; completed 2 years of core coursework and research.

University in Wuhan

2012.9 — 2015.6

Materials Physics & Chemistry | Master | 2012.9 — 2015.6

- Participated in NSFC and university-key R&D fund projects; 7 first-author papers (3 SCI, 1 EI, 3 Chinese core) on MPCVD high-quality diamond-film growth mechanisms; proficient with XPS, SIMS, AFM, FTIR and XRD characterization, and Origin/AutoCAD data modeling.

Key Projects

Project 1 — Advanced CMOS Film-Structure Optimization & Electrical Iteration

- With PIE/device teams, restructured the CVD film stack and interface-passivation plan to target short-channel effects, Vth drift, leakage and HCI reliability; used TCAD to predict process risk, iterated multiple device generations for logic/power production, and produced multiple device-class patents.

Project 2 — CVD New-Process Development & Device-Coherent Production

- Custom ALD/PECVD film processes for 3D NAND, LTPO and CMOS logic, solving step coverage, film stress and inter-layer mismatch; completed new-process DOE, reliability validation, pilot and full mass-production introduction, lifting overall yield and supporting long-term TD stability.

Project 3 — Process-Device Correlation Modeling & DFM (PhD Topic)

- Quantified how CVD thickness/composition/stress/interface-state variation affects MOS electricals and lifetime; built standardized simulation models; mapped layout/device-structure risks and output DFM specs, supporting PDK modeling, TD integration and front-end design.

Project 4 — Major Line-Defect Yield Ramp (PIE Collaboration)

- Resolved 3D NAND wafer arcing, PECVD particle bumps, TFT stress cracks and LTPO image-retention failures; via characterization + DOE located root causes, output standardized improvement recipes and SPC control, stabilizing line yield.

Intellectual Property

60+ first-author invention patents (5 granted, rest in substantive examination at CNIPA), spanning four directions:

Advanced CMOS/TFT/3D-memory novel device-structure design, and noise/leakage/long-term-reliability optimization;

PECVD/ALD novel film processes, composition control, step coverage and interface-passivation improvements;

Complete solutions to mass-production yield issues: film stress, particles, plasma discharge and surface defects;

Process-device co-adaptation, DFM optimization and device electrical-modeling innovations.